What is Claimed is:

[c1] A vertical PNP transistor comprising:

an emitter region including silicon and germanium.

[c2] The transistor of claim 1, wherein the maximum germanium concentration makes up no less than 10% of the silicon and germanium, and wherein the maximum germanium concentration makes up no more than 30% of the silicon and germanium.

[c3] The transistor of claim 1, wherein the silicon is a polysilicon.

[c4] The transistor of claim 1, wherein the transistor has a cutoff frequency greater than 1 GHz.

[c5] The transistor of claim 1, wherein the emitter region also includes carbon.

[c6] Vertical PNP and NPN transistors comprising:

a single layer of silicon that forms an emitter region of the PNP transistor, an extrinsic base region of the NPN transistor and an intrinsic base region of the NPN transistor.

[c7] The vertical PNP and NPN transistors of claim 6, wherein an emitter region of the PNP transistor includes silicon and germanium.

[c8] The vertical PNP and NPN transistors of claim 7, wherein the maximum germanium concentration makes up no less than 10% of the silicon and germanium, and wherein the germanium concentration makes up no more than 30% of the silicon and germanium.

[c9] The vertical PNP and NPN transistors of claim 7, wherein the emitter region also includes carbon.

[c10] The vertical PNP and NPN transistors of claim 7, wherein the silicon layer is polysilicon in the emitter region of the PNP transistor, and mono-crystal silicon in a portion of the extrinsic base region and mono-crystal silicon in the intrinsic base region of the NPN transistor.

[c11] The vertical PNP and NPN transistors of claim 6, wherein the PNP transistor has a cutoff frequency greater than 1 GHz.

[c12] A method of forming a PNP transistor while forming a CMOS device and an NPN transistor using at least two masking steps in addition to masking steps utilized in forming the CMOS and NPN devices, the method comprising:

a first masking step that defines a first opening through which implants for an intrinsic base and a collector of the PNP transistor are made; and

a second masking step that defines an emitter of the PNP transistor.

[c13] The method of claim 12, further comprising the step of implanting an n-type isolation through the first opening to separate the PNP collector from a substrate.

[c14] The method of claim 12, further comprising a third masking step that defines at least one opening through which an implant for an extrinsic base of the PNP is made.

[c15] The method of claim 12, further comprising the steps of:

depositing a layer of polysilicon over the second opening; and

growing an epitaxial layer of silicon and germanium,

wherein the silicon grows as a polysilicon over the polysilicon layer and as a mono-crystal silicon over the NPN.

[c16] The method of claim 15, further comprising the step of simultaneously forming the emitter of the PNP and an extrinsic base of the NPN by implanting p-type material.

[c17] The method of claim 16, wherein the emitter of the PNP includes silicon and germanium.

[c18] The method of claim 15, wherein the epitaxial layer also includes carbon.

[c19] The method of claim 15, further comprising the step of adding p-type material during the growing step.

[c20] The method of claim 15, wherein the polysilicon layer is no less than 10 nm,

and wherein the polysilicon layer is no more than 100 nm.